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IVT

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/431,477	11/01/99	GANESH K	884.141US1

021186
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P
1600 TCF TOWER
121 SOUTH 8TH STREET
MINNEAPOLIS MN 55402

MM21/0925

EXAMINER	
KIK,P	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/431,477	GANESH ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings filed on 11/1/1999 are acceptable under the new rules as being easily readable and scannable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-4,6-17,22-31** are rejected under 35 U.S.C. 102(b) as being anticipated by **Ito** (US Patent No. 5,648,910).

Ito (US Patent No. 5,648,910) discloses a method of automatically optimizing power supply network executed by a CAD systems and estimates current consumptions of component function blocks, taking into consideration electromigration problems (abstract; col. 4, lines 9-43; Fig. 2).

As per **claims 1-2,4,7-8,12,22-23,26-27,29-31**, all of the elements of the claims are illustrated in Fig. 2 (see also col. 4-7), wherein the iterative loops steps/means S7-S11 provides for the rearranging and analyzing steps/means, the layout rule defining a maximum current for a given width is part of step/mean S9, the reliability verification being electromigration is described

in abstract, and since the method is implemented by a CAD system (abstract), the memory, instruction, computer readable medium, and processor are inherently included.

As per **claims 3,6,9,11,13-17,24,25,28,** all of the elements of the claims are discussed in the rejection of claims 1-2,4,7-8,22-23,26-27,29-31 above, wherein the layout being a two-dimensional layout comprising a plurality of overlapping rows are further illustrated in Figs. 3-8, and the reliability consideration due to self-heating is associated with the electromigration as is well known in the art (see prior arts cited below).

As per **claim 10**, other layout considerations (i.e., layout/routing density) are also described in col. 4, lines 27-43.

4. **Claims 1-4,6-17,22-31** are rejected under 35 U.S.C. 102(b) as being anticipated by **Hathaway et al.** (US Patent No. 5,737,580).

Hathaway et al. (US Patent No. 5,737,580) disclose a method of wiring IC chips such that electromigration criteria are met while minimizing the effect on overall chip wireability, including optimizing wire width to adequately support the electromigration current on that net as a function of the capacitive loading of the net itself (abstract; Fig. 2; col. 3, line 1 to col. 5, line 67).

As per **claims 1-2,4,6-8,11-13,15,22-23,25-27,29-31**, all of the elements of the claims are illustrated in Figs. 2-4,6A,6B (see also col. 3, line 1 to col. 5, line 67), wherein the rearranging and analyzing steps/means is further described in col. 5, line 60 to col. 6, line 5, wherein the overlapping rows are inherently included as part of the routing/placement problems that often

occurs as is well known in the art, and since the method is implemented by a CAD system (i.e., EDA tools--col. 1, lines 5-12), the memory, instruction, computer readable medium, and processor are inherently included.

As per **claims 3,9,14,16,17,24,28**, the reliability consideration due to self-heating is associated with the electromigration check as described in col. 5, lines 25-59 wherein such self-heating is always associated with electromigration as is well known in the art (see prior arts cited below).

As per **claim 10**, other layout considerations (i.e., routing complexity--detailed and global routing; timings) are also described in col. 4, line 31 to col. 5, 25.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ito** (US Patent No. 5,648,910).

As per **claim 5, Ito** discloses all of the elements of the claim as discussed in the rejection of claim 1 above, but failed to particularly teach that the circuit design be a microprocessor

design. However, it would have been obvious to one of ordinary skilled in the art at the time of the invention that the circuit design method/apparatus of **Ito** is also applicable to microprocessor design since microprocessor design are also subjected to electromigration problems due to similar technologies as is well known in the art in which the method/apparatus of **Ito** can be applied.

7. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hathaway et al.** (US Patent No. 5,737,580).

As per **claim 5**, **Hathaway et al.** disclose all of the elements of the claim as discussed in the rejection of claim 1 above, but failed to particularly teach that the circuit design be a microprocessor design. However, it would have been obvious to one of ordinary skilled in the art at the time of the invention that the circuit design method/apparatus of **Hathaway et al.** is also applicable to microprocessor design since microprocessor design are also subjected to electromigration problems due to similar technologies as is well known in the art in which the method/apparatus of **Hathaway et al.** can be applied.

8. **Claims 18-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hathaway et al.** (US Patent No. 5,737,580) in view of **Gupta et al.** ("Optimal 2-D cell layout with integrated transistor folding", 1998 IEEE/ACM International Conference on Computer-Aided Design, 8 November 1998, pp. 128-135).

Gupta et al. disclose a technique that integrates folding into the generation of optimal layouts of CMOS cells in the two dimensional style to optimize some cost function under a set of constraints such as cell area and/or delay optimization (abstract; sections 3-6).

As per **claims 18-21, Hathaway et al.** disclose all of the elements of the claims as discussed in the rejection of claim 14 which the claims depend. However, **Hathaway et al.** failed to further teach the adjusting of one or more of the components in one of the clusters to comply with a size constraint (i.e., device-based legging, stack-based legging, differential legging). Such methods for further compacting the transistors is well known in the art as further taught by **Gupta et al.** to further optimize the cells of the pluralities of integrated circuit components under a set of constraints (abstract; sections 2-6). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the compacting/transistor folding method of **Gupta et al.** into the system/method of **Hathaway et al.** because such compacting/transistor folding method would further optimizes the integrated circuit components cell layouts as is well known in the art.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicants are requested to carefully consider them in response to this Office Action. In particular, the following prior arts made of record are most relevant:

Basaran, B. Et al., ("GeneSys: A Leaf-Cell Layout Synthesis System for GHz VLSI Designs", Proceedings of the 12th International Conference on VLSI Design, pp. 448-452, January 1999) teach that the layouts generation involving device resizing, and/or deleting devices or legs as necessary, can also be used for process migration (section 2; page 449, last paragraph).

Riepe, M.A., et al., ("An Efficient Level Micro Placement and Routing for Two-Dimensional Digital VLSI Cell Synthesis", Technical Report CSE-TR-364-98, The University of Michigan, Ann Arbor, pp. 1-18, June 1998) discloses layout clustering followed transistor folding and stack generation (sections 2.1 and 2.2).

10. The following are other prior arts not relied upon but are considered pertinent to applicant's disclosure. Therefore, Applicants are requested to carefully consider them in response to this Office Action.

Young et al. (US Patent No. 6,038,383) disclose a method for design and fabricating an integrated circuit wherein signal line interconnect widths are determined by performing an electromigration analysis on a trial layout of the integrated circuit (abstract; col. 2, lines 1-59; col. 4, lines 1-67).

Gardner (US Patent No. 5,817,574) discloses a method of forming a high surface area interconnection structure, taking into consideration reliability factor such as electromigration and self-heating problems (abstract; col. 1, lines 42-57; col. 4, lines 16-67).

Kazami (US Patent No. 6,242,807) discloses a semiconductor integrated circuit having heat sinking means for heat generating wires for high reliability circuit design (abstract; col. 2, lines 21-46).

Buch (US Patent No. 6,253,361 B1) discloses a method for designing a sequence of logic gates in a path, including adjustment to electrical components such as cell selection and sizing to

overcome the delays and maintains signal integrity (abstract; col. 1, lines 20-33; col. 3, line 52 to col. 4, line 15).

Peleggi et al. (US Patent No. 6,286,128 B1) disclose a method for design optimization using logical and physical information, including routing that takes into consideration signal delay and integrity, current density and electromigration (abstract; col. 6, lines 45-67; col. 9, line 50 to col. 10, line 27).

Gupta (US Patent No. 6,163,877) discloses a computer implemented method for generating a layout for a set of transistors on a semiconductor chip, the method comprising the step of folding transistors of the set whose sizes exceed a predetermined maximum size which includes generating diffusion sharing arrangements that are unique with respect to transistor folds, transistor orientations, and transistor fold interlacing arrangement (abstract; Fig. 9).

Carter et al. (US Patent No. 6,077,308) disclose a method and system for constructing polygon layout, wherein transistor folding is applied to the symbolic representation generated from a schematic to meet the cell height constraints (abstract; col. 3, line 55 to col. 4, line 67).

Saika (US Patent No. 5,995,734) discloses a method for determining transistor placement of a cell by grouping/clustering the transistors with common connectivities and performing transistor folding, taking into consideration wiring density (abstract; col. 3, line 60 to col. 6, line 67).

Maziasz et al. (US Patent No. 5,737,236) disclose an apparatus/method for the automatic determination of a standard cell library height within an integrated circuit design, wherein the

method selects an optimized standard cell height within an integrated circuit design, wherein the differing cell structures for a single cell type includes different transistor folding combinations, different element placements within the cell structure, different element or transistor aspect ratios and different routing between elements within the cell structure (abstract; col. 4, lines 5-56).

Aoki (US Patent No. 5,675,501) discloses a method of design a semiconductor integrated circuit having no dead space wherein a placement step of generating row information indicating a transistor row in which transistors required for the configuration of a transistor to be designed are placed so that wiring length is as short as possible, including performing transistor folding in the x and y direction to meet the required wiring length and size criteria (abstract; Fig. 3; col. 5, line 21 to col. 9, line 59).

Frost et al. ("RELIANT: a reliability analysis tool for VLSI interconnects", Proceedings of the IEEE 1988 Custom Integrated Circuits Conference, 16 May 1988, pp. 27.8/1-27.8/4) disclose a CAD tool which predicts the failure rate of integrated circuit conductors using circuit layout, device models, and electromigration process data (abstract; pages 27.8/2-3).

Liew et al. ("Circuit reliability simulator for interconnect, via, and contact electromigration", IEEE Transactions on Electron Devices, Vol. 39, No. 11, November 1992, pp. 2472-2479) disclose a simulator that generate layout advisory for width and length of each interconnect, and the number of contacts and vias at each node in a circuit and estimate the overall circuit electromigration failure rate and/or cumulative percent failure as functions of time, temperature, voltage, frequency and previous stress (abstract; sections III-IV).

Teng et al. ("iTEM: a temperature-dependent electromigration reliability diagnosis tool", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 8, August 1997, pp. 882-893) disclose an electromigration reliability diagnosis tool for CMOS VLSI circuits which can estimate the interconnect temperature rise due to joule heating and heat conduction from the substrate using lumped thermal model (abstract; section V).

Surkan ("Design for a Network-Based Education System that Evolves by Peer and Instructor Interaction", 1998 Proceedings of IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2 November 1998, pp. 275-279) disclose a method for electromigration reliability enhancement technique using automatic wire widening wherein minimum layout perturbation criteria is used when adjusting the positions of layout elements to preserve as much structure of the layout as possible (abstract; section 2).

Chowdhury et al. ("Optimum design of IC power/ground nets subject to reliability constraints", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 7, No. 7, July 1988, pp. 787-796) disclose a method that formulates and solves the problem of sizing power/ground nets in integrated circuits composed of mules, wherein the nets are routed as trees in the channels between modules, wherein the objective is to minimize the area of the power/ground nets subject to the constraints which were developed to maintain proper logic levels and switching speed, to prevent electromigration, and to satisfy certain rule requirements (abstract; sections 2-3).

Dalal et al. ("Design of an efficient power distribution network for the UltraSPARC0I microprocessor", Proceedings of 1995 IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2 October 1995, pp. 118-123) disclose the design, implementation and verification of the power distribution network for the 5.2 million transistor UltraSPARC-I microprocessor wherein a simulation method allows rapid identification of exact layout locations with potential electromigration or excessive voltage drop problems (abstract; sections 3-5).

Wolf et al. ("Reliability driven module generation for analog layouts", Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, Vol. 6, 30 May 1999, pp. 412-415) disclose a reliability driven module generation for analog layouts wherein the reliability of analog layouts is improved by an automatic check of electrical constraints like electromigration and voltage drop due to interconnection resistances after the modules have been generated (abstract; sections 2-4).

Van Genneken et al. ("Doubly folded transistor matrix layout", IEEE International Conference on Computer-Aided Design, 7 November 1988, pp. 134-137) disclose a flexible module generator that lays out transistor net lists as a two-dimensional folding problem (abstract; sections 3-4).

Her et al. ("Cell area minimization by transistor folding", Proceedings of European Design Automation Conference, 20 September 1993, pp. 172-177) disclose a method for folding transistors wherein two rows of transistors, one for P-type transistors and the other for N-type

transistors, and attempt to determine an optimal folding for each transistor to minimize the layout area (abstract; sections 2-5).

Gupta et al. ("XPRESS: a cell layout generator with integrated transistor folding", Proceedings of European Design and Test Conference, 11 March 1996, pp. 393-400) disclose a method for generating area-efficient layouts of complex CMOS cells in the one-dimensional (linear) style) including transistor sizing via folding technique which integrates folding into the synthesis algorithms and optimal diffusion sharing (abstract; section 3).

Kim et al. ("An Efficient Transistor Folding Algorithm For Row-based CMOS Layout Design", Proceedings of the 34th Design Automation Conference, 9 June 1997, pp. 456-459) disclose an efficient algorithm to find the optimal transistor folding sizes in row-based designs (abstract; section 3).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is (703) 306-3039. The examiner can normally be reached on Monday to Thursday from 8:30 AM to 6 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith, can be reached at (703) 308-1323. The fax phone number for this Group is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1782.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-3431, (for formal communications intended for entry)

Or:

(703) 746-4111 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and please inform the Examiner prior to faxing)

Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

PK

September 18, 2001

Vuthe Siek

VUTHE SIEK
Patent Examiner